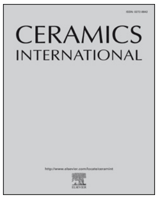
Ceramics International 46 (2020) 23433–23441

Contents lists available at ScienceDirect

Ceramics International

journal homepage: www.elsevier.com/locate/ceramint



Double pentavalent (Sb^{5+}, Nb^{5+}) and trivalent (Sm^{3+}, Y^{3+}) co-doped $Ti_{0.9}Zr_{0.1}O_2$ colossal dielectric permittivity multilayer ceramics for the miniaturization of the next-generation electronics

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ARTICLE INFO

Keywords:
Double co-doped TiO_2
Colossal dielectric permittivity
Multilayer ceramics
DC bias

ABSTRACT

Materials with colossal dielectric permittivity (CP) are in the focus of interest for the development of miniaturization and integration of electronic components. Despite the extensive study of these new classes of co-doped TiO_2 CP materials, the preparation of multilayer ceramics using this kind of CP materials is still challenging work. Here, we synthesize a series of (Sb^{5+}, Nb^{5+}) and (Sm^{3+}, Y^{3+}) co-doped $Ti_{0.9}Zr_{0.1}O_2$ ceramics (SNSYTZO) through the conventional solid-state reaction method. XRD spectrum identifies that ceramics under $x = 0.04$ show a perfect rutile phase with the tetragonal crystal structure; however, minor brookite orthorhombic crystal structure appears when $x > 0.04$. FESEM images show the prepared ceramics have excellent densification and low porosity. Dielectric, modulus, and impedance spectrum are systematically explored the underlying CP mechanism and compared with each other to find the optimal materials composition to prepare further multilayer ceramics, which is fabricated by the industrial tape casting method. FESEM, together with surface element mapping, indicates that all doping elements are homogeneously distributed. Also, we investigate the dielectric response without/with DC bias. This work sheds light on a promising feasible route to prepare the miniaturization of the next-generation electronics via a large scale industrial tape casting method.

1. Introduction

The requirements for miniaturization and integration of modern electronic components are constantly increasing, making the exploration of colossal dielectric permittivity ($\varepsilon' > 10^4$) materials a hot topic in the field of new dielectric materials design. Colossal dielectric permittivity (CP) materials have demonstrated their excellent dielectric and energy storage characteristics with extremely high dielectric permittivity. These CP materials can be profoundly used in developing the small-sized, large-capacity capacitors and high-energy storage devices in electric vehicles, mobile electronics, aerospace, and military, which has attractive application prospects [1]. Existing CP materials include $CaCu_3Ti_4O_{12}$ (CCTO) [2], $Ba(Fe_{0.5}Nb_{0.5})O_3$ [3], $La_{15/8}Sr_{1/8}NiO_4$ [4], doped $BaTiO_3$ [5], doped NiO [6], however, the shortcomings existing in these material systems still hinder their wide application in dielectric capacitors and other fields. For example, the dielectric response of the doped $BaTiO_3$ system has a strong temperature dependence, which limits the development and application of the material system in a wide temperature range. CCTO exhibits CP response in a broad temperature (150–400 K) and in wide frequency ($< 10^7$ Hz) range. However, its high dielectric loss and low breakdown field strength limit its development and application of energy storage and overvoltage protection. The existing CP materials maybe meet the requirements of device miniaturization in terms of dielectric constant, however, their corresponding low withstand voltage characteristics, low temperature stability, and high dielectric loss have hindered the development and application of devices [7].

The (Nb + In) co-doped rutile TiO_2 as a new CP material through

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https://doi.org/10.1016/j.ceramint.2020.06.113
Received 27 February 2020; Received in revised form 13 May 2020; Accepted 10 June 2020

defect chemistry design found by Hu et al. [8] illustrates a high dielectric permittivity ($\sim 10^5$), the important thing is that the material has a low dielectric loss ($< 5\%$) in the broader temperature (80–450 K) and frequency ($< 10^6$) range. Here, polar clusters are attributed to the main factor affecting the dielectric mechanism, as a result of this, the "electron-pinned defect-dipole" (EPDD) dielectric response mechanism is proposed. A small amount of co-doping could form a diamond coordination structure of $Nb_2^{5+}Ti^{3+}ATi$ ($A = Ti^{3+}/In^{3+}/Ti^{4+}$) and triangle-coordinated $In_2^{3+}V_O^{\cdot\cdot}Ti^{3+}$ local defect structure, suppressing polarons or oxygen vacancies generated by a single doped Nb^{5+} or In^{3+}, without reducing the dielectric permittivity and low loss are achieved at the same time. This new materials design provides a new idea for CP and low dielectric loss materials. Meanwhile, the dielectric response of this co-doped TiO_2-based material system makes it much more attractive for capacitor miniaturization and high energy density storage. Thus, research on this material system has been carried out rapidly.

The EPDD polarization mechanism then shows its successful application in 2014, Gai et al. [9] prepared the amorphous thin film of (Nb + In) co-doped TiO_2 material system, which exhibits a dielectric constant of approximate 4000 and a dielectric loss of around 5%. In the same year, Li et al. [10] repeated the CP properties of this materials system, however, proposing that the CP properties of this materials system may mainly originate from the non-intrinsic contribution, i.e., internal barrier layer capacitor (IBLC) effect, rather than the intrinsic EPDD effect. In 2015, Wu et al. [11] did lots of research work and prepared a series of (Bi, Pr, Dy, Sm, Gd, Yb, Ga, Al, Sc) doped ceramics, showing that Bi-doped TiO_2 ceramics exhibit the high dielectric constant (4.2×10^4) with the acceptable dielectric loss (8.3%), a good temperature (−125 to 200 °C) and a frequency (10^2–10^6 Hz) stability. The dipole polarization mechanism in those CP materials all attributed to EPDD effect. In 2016, Kawarasaki et al. [12] fabricated the (Nb + In) co-doped TiO_2 single crystal, whose CP (8×10^4) temperature range extends to an ultralow temperature value of 25 K. It is considered that a complex defect structure is the cause of this CP phenomenon. In 2017, Liu et al. [13] sintered the (Yb + Nb) co-doped TiO_2 ceramic and found that its dielectric permittivity is above 10^4 (tested under 10^6 Hz). After carefully studied the effect of oxygen partial pressure during sintering process on ceramic grains, dielectric properties and breakdown field strength, their work definitely verify that the concentration and type of the defects structure have an immense influence of dielectric properties and breakdown field strength in co-doped TiO_2 CP material system. From the point of view of dielectric spectroscopy, in 2018, Petzelta et al. [14] presented the dielectric spectra from sub-Hz to THz. They modelled the dielectric spectra as a composite of IBLC and surface barrier layer capacitor (SBLC). In 2019, Yang et al. [15] fabricated the (Ta + Ag) co-doped TiO_2 ceramics and simultaneously realized a broad temperature stability range (temperature coefficient of dielectric permittivity range from 6.8% to 8.8% in range of −200 to 200 °C) and outstanding dielectric performance, dielectric permittivity of approximate 9831 and a very low dielectric loss of approximate 0.041 under 1k Hz test frequency, which meet the requirement of the commercial X9R capacitor (temperature coefficient of dielectric permittivity within 15% range from −55 to 200 °C).

In our previous study, we have prepared CP (Nb + In) co-doped TiO_2 ceramics, and systematically investigate their phase structure, morphology microstructure, annealing effect, chemical valence state of elements, dielectric response as a function of temperature and frequency with/without bias, complex modulus analysis, impedance spectrum simulation, microelectrodes I–V within and across grain test, secondary phase SiO_2 doping to decrease the dielectric loss and improve breakdown strength, different A-site, and B-site ZrO_2 doping trial to optimize materials composition [10,16–21]. We ascribe the CP machoism to IBLC effect in medium frequency (10–10^6 Hz) base on aforesaid work. Therefore, we try to put this material system to a commercial capacitor and find its acceptable applications.

Here, we want to propose double doping means to achieve a high-performance dielectric response. Some conventional test is employed to character its phase structure and morphology structure. The dielectric and modulus versus frequency and temperature are systemically investigated to find the acceptable material composition to meet the multilayer ceramics process. Impedance spectrum as a power tool is employed to analysis various activation energy and vindicate CP mechanism. Meanwhile, we prepare the multilayer ceramics of this materials system using the industrialized tape casting method. The morphology and element distribution analysis indicates the excellent quality of prepared multilayer ceramics with high density and low porosity, without delamination, sintering crack, and inner electrode migration. From the application viewpoint, we investigate the dielectric response versus frequency and temperature with/without bias applied, respectively. This consistent work could break through log-jam associated with the industrial large scale processing and application of co-doped TiO_2 CP materials and put forward the development of miniaturization of electronic capacitors.

2. Experimental section

The solid solutions $x(Sb_{0.5}Nb_{0.5})$-$x(Sm_{0.5}Y_{0.5})$-$(1\text{–}2x)(Ti_{0.9}Zr_{0.1})O_2$ [$x = 0, 0.01, 0.02, 0.04, 0.06, 0.08, 0.1, 0.2$] (Abbr. as SNSYTZO) were first prepared by classical solid-state ways using rutile TiO_2 (99.9%), ZrO_2 (99.9%), Sb_2O_5(99.95%), Nb_2O_5 (99.95%), Sm_2O_3 (99.95%), and Y_2O_3 (99.9%) as raw material. The mixed powders were mixed with milling for 48 h to get a homogenous mixing with fine grains. After mixing, the powders were drying off the water in the oven. The powders with 1 wt% PVA were pressed into tablet-like samples. To achieve high-density ceramics, those samples ($x = 0$, 0.01, 0.02, and 0.04) were treated in the high-temperature furnace 1550 °C with 4h dwelling time, samples ($x = 0.06$ and 0.08) were sintered at 1450 °C with 4h dwelling time, and samples ($x = 0.1$ and 0.2) were sintered at 1350 °C with 4h dwelling time. Then the samples were coated with silver paste and fired at 550 °C for 0.5 h to burn out the organic additives. The prepared ceramics with silver electrodes were used to investigate the systemic electric properties. After selecting the suitable materials composition, we repeated the mixed powder processing. However, the powder was weighted according to the stoichiometric ratio and mixed for a long-time (7 days) with 1 wt% sintering aids ($0.1Bi_2O_3$-$0.2B_2O_3$-$0.6SiO_2$-$0.1Li_2O$) to refine the powder size to around 200 nm. Then the powders were using water-based tape-casting organic additives to tape cast, using polyacrylic acid, polymethacrylic acid, and ammonium polyacrylate as a dispersant, polyvinyl acetate, polyacrylate, and polyvinyl acetate as a binder, polyethylene glycol, polypropylene glycol, and glycerol as a plasticizer. The fine powders with the mixed dispersant were first added to the bottle for 48 h milling, then added the mixed binder to mill another 48 h, finally added the plasticizer to mill for 48 h to get solvent, which would be used to fabricate the thick films by tape casting. SNSYTZO thick films with inner printed platinum electrodes were stacked layer by layer, and then precisely first aligned with cold lamination at a value of 60 °C and 200 PSI, then warm water isostatic pressure at a value of 75 °C and 3000 PSI. Finally, the stacked layers were sintered range from 1100 °C to 1330 °C. After sintering, room-temperature quick-drying silver glue was pasted to terminate the opposite ends and form side electrodes for the further dielectric measurements.

To explore the microstructure and further optimize the composition of CP ceramics, a series of analysis were carried out. The samples' phase structure was investigated with X-ray diffractometer (XRD, Rigaku D/MAX 2400, Japan) equipped with Cu $K\alpha$ radiation ($\lambda = 1.54$ Å) under a scan step of 0.02°. The field-emission scanning electron microscopy (FESEM, FEI NanoSEM 630) energy-dispersive X-ray analysis (EDX) was employed to morphology microstructure and element distribution of the ceramics. The dielectric response at room temperature of samples were tested by E4980A (Agilent, USA). In addition, the systemic dielectric, modulus, and impedance properties were explored using a

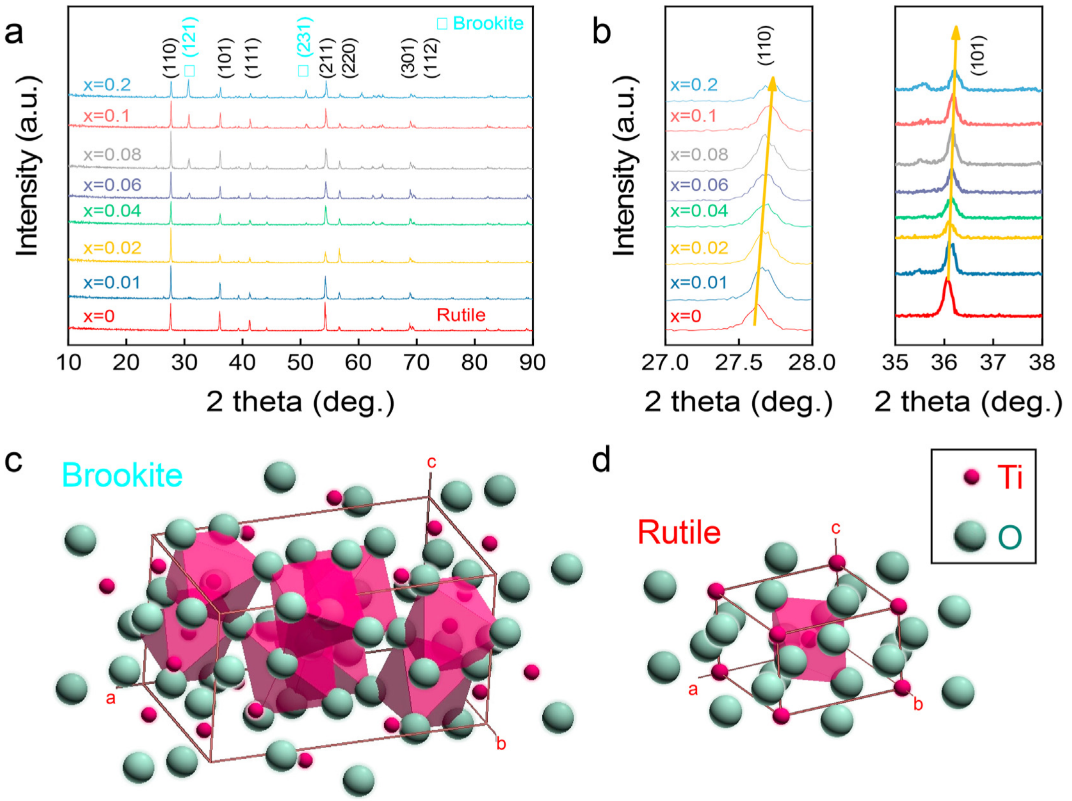

Fig. 1. (a) XRD patterns for the selected co-doped SNSYTZO ceramics, (b) The enlarged view of XRD patterns to show the variation of diffraction plane peaks. (c) The schematic diagram for the Brookite crystal structure of the orthorhombic crystal system with space group Pbca. (d) The schematic diagram for the Rutile crystal structure of the tetragonal crystal system with space group $P4_2/mmm$.

broadband dielectric spectrometer E4980AL (Agilent, USA) with the frequency range of 4–110M Hz, the bias range 0–100V, a temperature range of −150–250 °C (PolyK, USA).

3. Results and discussion

To analysis the phase microstructure, influencing macroscopic dielectric performance, Fig. 1 displays the XRD patterns of different SNSYTZO [x = 0, 0.01, 0.02, 0.04, 0.06, 0.08, 0.1, 0.2] ceramics in the 2θ range from 10 to 90°, revealing that samples under $x \leq 0.04$ were in pure rutile structure. However, minor secondary brookite phases appear when $x \geq 0.06$. The main phase of rutile TiO_2 (PDF#97-003-1322) is applied to identify all diffraction plane of the prepared ceramics, indicating that double pentavalent (Sb^{5+}, Nb^{5+}) and trivalent (Sm^{3+}, Y^{3+}) with Zr^{4+} ions are in a rutile crystal host lattice despite the minor accompanying brookite TiO_2 (PDF#97-007-7693) crystal structure, as shown in Fig. 1 a. Meanwhile, with increasing pentavalent (Sb^{5+}, Nb^{5+}) and trivalent (Sm^{3+}, Y^{3+}) doping concentration, the diffraction plane (110) and (101) peaks slowly shift to high angles, as displayed in Fig. 1 b, indicating the reduction of d-spacing according to the classical equation $2dSin\theta = \lambda$. Meanwhile, Fig. 1c and d give the schematic diagram of both brookite and rutile crystal structure, respectively.

To illustrate the morphology evolution with increasing doping concentration of double pentavalent (Sb^{5+}, Nb^{5+}) and trivalent (Sm^{3+}, Y^{3+}) of $Ti_{0.9}Zr_{0.1}O_2$ ceramics, we present their SEM images and the related statistic of grain size distribution, as shown in Fig. 2 a to h. The morphology microstructures present that all samples have a relatively high density and are almost independent of the doping ions. The mean grain size of SNSYTZO slightly reduces from 30 μm to 23μm with increasing doping ions according to the right-corner inset graph, as shown in Fig.2 a to h, always attributing to the conventional ions pinning effect impeding the mobility of grain boundary during the high-temperature sintering process [22,23]. Meanwhile, it is noted that the bigger the mean grain size, the higher the SD value. The SD decrease from the value of 12 to 5, i.e., the grain size becomes uniform with the increase of doping ions. The reason could also attribute to the secondary phases pinning effect [24], which also restricts the growth of crystal grain.

To explore the effect of double pentavalent (Sb^{5+}, Nb^{5+}) and trivalent (Sm^{3+}, Y^{3+}) of $Ti_{0.9}Zr_{0.1}O_2$ ceramics, we first tested their dielectric permittivity and loss as a function of frequency range from 10 to 1k Hz at room temperature, as shown in Fig. 3 a to d. The dielectric permittivity of un-doped slightly declines from 55 (under 20 Hz) to 47 (under 1k Hz), while the dielectric loss sharply decreases 1.39 (under 20 Hz) to 0.08 (under 70 Hz), then slowly down to 0.04 (under 1k Hz), as shown in Fig. 3 a. The high dielectric loss in the range of low frequency (< 100 Hz) could be attributed to the space charge dissipation effect [25]. Surprisingly, the dielectric permittivity drastically augments to a frequency-independent value 10^4 from 55 when doping x = 0.01 double pentavalent (Sb^{5+}, Nb^{5+}) and trivalent (Sm^{3+}, Y^{3+}) ions to $Ti_{0.9}Zr_{0.1}O_2$ ceramics. The dielectric loss remarkably reaches to around 1 during the whole test frequency range, as presented in Fig. 3 b. However, the dielectric permittivity goes up to 10^5 (under 20 Hz), and dielectric loss decrease to 0.17 (under 20 Hz) with increasing doping content to x = 0.02, as shown in Fig. 3 b. Meanwhile, the dielectric loss slightly increases to 0.6 (under 1k Hz) and shows the frequency dependence. With increasing doping content to x = 0.04, the dielectric permittivity nearly keep the same value 10^5. However, the dielectric loss significantly decreases to 0.06 (under 20 Hz), as illustrated in Fig. 3 c. The dielectric loss of x = 0.04 SNSYTZO ceramics slightly achieves to 0.1 with increasing test frequency, simultaneously, the dielectric permittivity down to 2.8×10^4, which is still much larger than the un-doped compositions. However, their dielectric loss goes up with increasing doping content x = 0.06 to 0.2 despite their dielectric

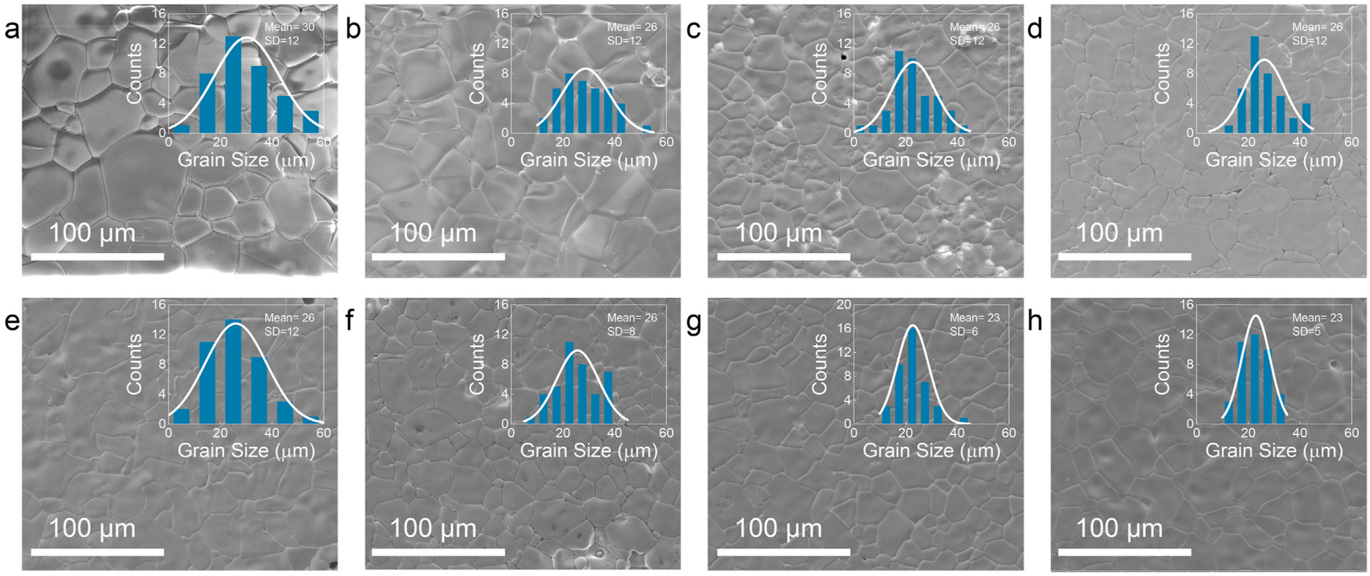

Fig. 2. FESEM images of the selected x($Sb_{0.5}Nb_{0.5}$)-x($Sm_{0.5}Y_{0.5}$)-(1−2x)($Ti_{0.9}Zr_{0.1}$)O_2 ceramics with (a) x = 0, (b) x = 0.01, (c) x = 0.02, (d) x = 0.04, (e) x = 0.06, (f) x = 0.08, (g) x = 0.1, and (h) x = 0.2. The right-corner inset of each SEM image is the related grain size distribution. The “Mean” stands for the average size of each ceramics. The “SD” refers to the standard deviation of grain size.

permittivity keep the same level, as shown in Fig. 3 c and d. The variation tendency of dielectric loss could be attributed to the weekly-localized defect-dipoles according to the EPDD theory in these SNSYTZO series ceramics [8]. As we could find the dielectric loss at 1000 Hz decrease from 1.08 (x = 0.01) to 0.19 (x = 0.04), and then goes up to 0.699 (x = 0.1), meanwhile, in Fig. 1 a, the XRD results show the second phase brookite appear when x > 0.04. Here, we think the EPDD structure slightly increase in the rutile phase, which would

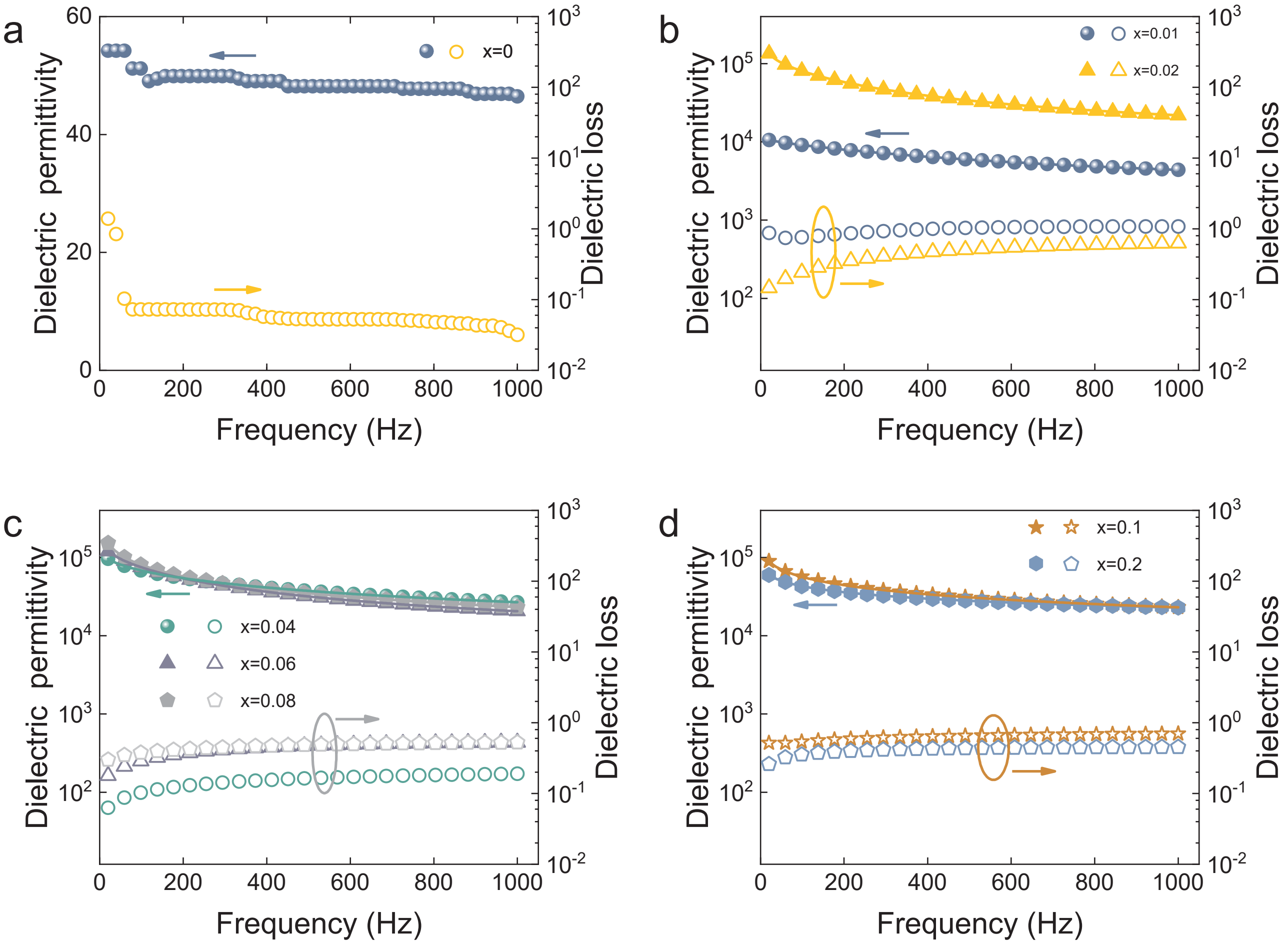

Fig. 3. Dielectric permittivity and loss versus frequency range from 10–1000 Hz at room temperature for the selected SNSYTZO ceramics.

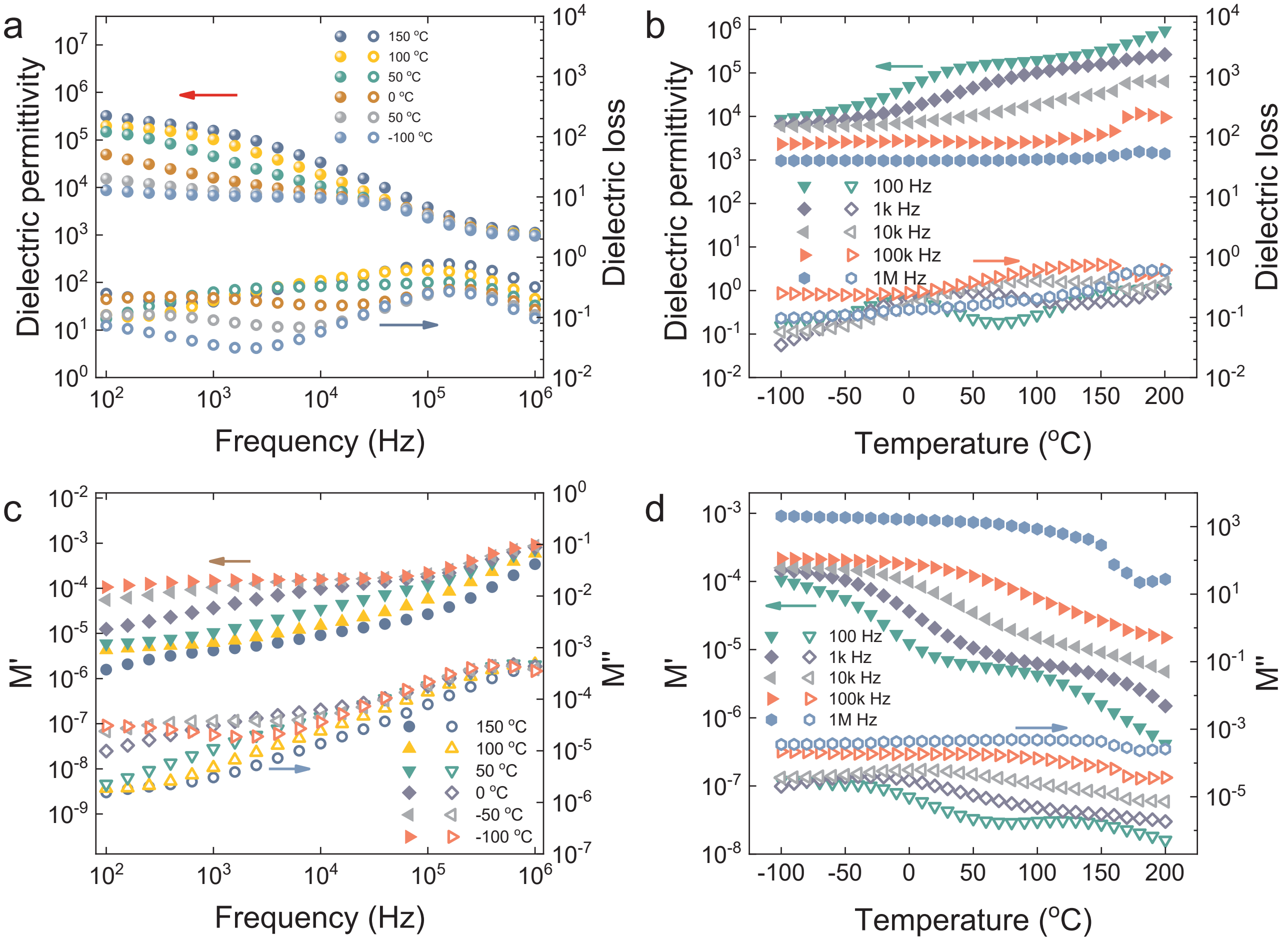

Fig. 4. (a) The dielectric permittivity and loss as a function of frequency with the selected temperature (−100, −50, 0, 50, 100, and 150 °C) for x = 0.04 SNSYTZO ceramic. (b) The dielectric permittivity and loss versus temperature with the selected frequency (100, 1k, 10k, 100k, and 1 M Hz) for x = 0.04 SNSYTZO ceramic. (c) The real and imaginary part of modulus of x = 0.04 SNSYTZO ceramic dependence of frequency at a selected temperature (−100, −50, 0, 50, 100, and 150 °C). (d) The real and imaginary part of modulus of x = 0.04 SNSYTZO ceramic versus temperature range from −100 to 200 °C at selected temperature frequency (100, 1k, 10k, 100k, and 1 M Hz).

hinder the weekly-localized electron and decrease the dielectric loss when $x \leq 0.04$. However, when the brookite phase appears, those EPDD structures may not arrange orderly to impede the weekly-localized electron so that the dielectric loss largely increase when $x > 0.04$.

Base on aforesaid dielectric behavior test, we take the x = 0.04 SNSYTZO ceramic to investigate the dielectric permittivity and loss further versus temperature under the selected frequency, as shown in Fig. 4 a and b, take into consideration that the dielectric loss is a crucial factor for describing the energy dissipation and could cause the temperature rise of device. The dielectric permittivity increase with increasing test temperature in the frequency range from 100 to 10^5 Hz, while remaining uncharged above 10^5 Hz, as shown in Fig. 4 a. This increase in dielectric permittivity with the temperature at lower frequency is due to the enhanced mobility of thermally generated charge carriers [26], which will loosen the pinning effect of weekly-localized defect-dipoles [8]. The invariable dielectric permittivity with the temperature at high frequency could be to the reason that the delocalized defect-dipoles could not keep up with the extra test frequency. The dielectric loss reaches a relaxation peak around 10^5 Hz, corresponding to the change of dielectric permittivity plateau, and it is a typical Debye dielectric relaxation behavior. Notably, the dielectric loss does not exhibit large dispersion in the low-frequency range, indicating that there was no extra non-Debye dependence, such as electrode-ceramic polarization and/or space charge polarization. Fig. 4 b clearly shows that the dielectric permittivity decrease with increasing test frequency during the whole test temperature range from −100 to 200 °C. And the dielectric permittivity under high frequency has better temperature stability than that under low frequency.

To exclude the conductivity process hides in a dielectric relaxation behavior dependence of temperature and frequency, modulus [27], as an excellent method to probe, interpret, and analyze the dynamical aspects of electrical transport phenomena, is employed to give an insight into the electrical processes. Complex modulus M* is written as $M^* = 1/(\varepsilon' - i\varepsilon'') = \varepsilon'/(\varepsilon'^2+\varepsilon''^2) + i\varepsilon''/(\varepsilon'^2+\varepsilon''^2) = M' + iM''$, where ε', ε'', and i are real and imaginary part of complex dielectric permittivity and $\sqrt{-1}$, respectively, meanwhile, $M' = \varepsilon'/(\varepsilon'^2+\varepsilon''^2)$ and $M'' = \varepsilon''/(\varepsilon'^2+\varepsilon''^2)$ are defined as the real and imaginary part of complex modulus. Fig. 4 c and d illustrate the variation of the real and image part of modulus with frequency/temperature at different temperature/frequency (−100, −50, 0, 50, 100, and 150 °C)/(100, 1k, 10k, 100k, and 1 M Hz) for the x = 0.04 SNSYTZO ceramic. Both modulus spectrum at low frequency has no obvious peak, indicating the lack of conductance and related conductance polarization effect [28]. The prepared ceramics here have excellent insulate characteristics to prove the further dielectric test and practical application.

To evaluate the activation energy, and obtain insight into the dielectric relaxation behavior of x = 0.04 SNSYTZO dielectrics, the impedance spectrum is investigated during the temperature range from −100 to 200 °C, as shown in Fig. 5 a to e. The complex impedance Z*

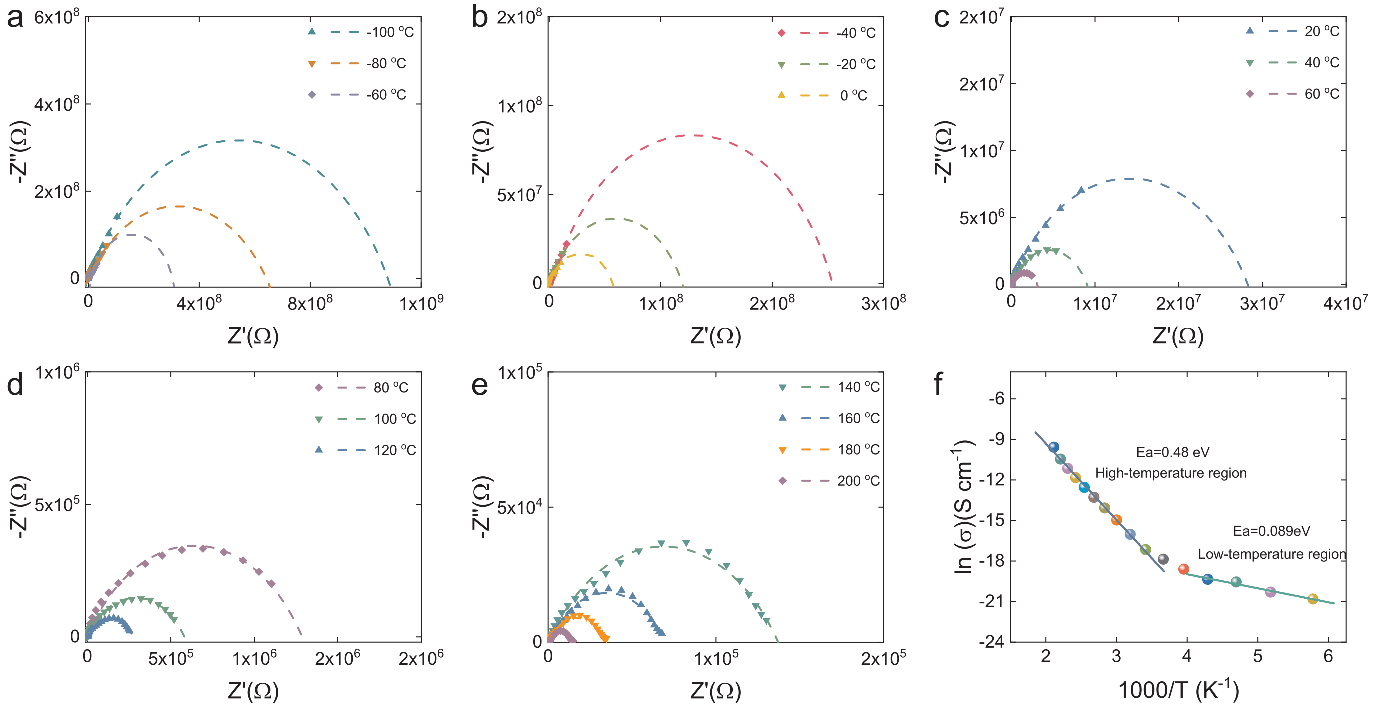

Fig. 5. Cole–Cole draw plotted Z′(ω) as abscissa axis and -Z''(ω) as ordinate for x = 0.04 SNSYTZO ceramic range from −100 to 220 °C. (a) −100 to −60 °C. (b) −60 to 0 °C. (c) 20–60 °C. (d) 80–120 °C. (e) 140–200 °C. (f) The DC conductivity dependence of temperature for this studied sample. The solid lines are the best linear fitting data to the solid experimental symbols, according to Arrhenius law.

are written as, $Z^* = Z'\text{-}iZ'' = R/[1+(\omega\tau)^2]\text{-}iR\omega\tau/[1+(\omega\tau)^2]$, where Z′ the real part of the complex Z*, -Z″ the imaginary part of complex Z*, R the ceramics' resistance, C the capacitance of ceramics, the relaxation times τ equal to RC, angular frequency ω equal to 2πf. When we get rid of R, τ, and ω, the equation could be rewritten as $(Z'\text{-}R/2)^2+Z''^2=(R/2)^2$, and it is the typical Cole-Cole draw arc [28,29]. Clearly, only one arc appears in the whole temperature range. Meanwhile, the resistance of this study samples drastically decreases from the order of 9 to 5 with increasing temperature from −100 to 200 °C, as displayed in Fig.5 a to e, indicating a thermally activated resistance. The resistance dependence of temperature follows a classical Arrhenius law [30], $\sigma = \sigma_0\exp(\text{-}E_a/K_BT)$, where σ_0 a constant, E_a the activation energy, K_B the Boltzmann constant, and T the absolute temperature. Fig. 5 f presents the DC conductivity dependence of temperature for this studied ceramic. The activation energies for the high and low-temperature regions are calculated 0.48 eV and 0.089 eV, respectively. The 0.089 eV of this studied ceramic could be attributed to the intrinsic electron traps in shallow potential due to the electron pinning effect, which should be associated with the CP phenomenon of x = 0.04 SNSYTZO ceramic. However, the 0.48 eV here is associated with oxygen vacancy or an interfacial process, such as traditional Maxwell-Wagner effects [31]. Return to Fig. 4 b, the dielectric permittivity at low frequency and high temperature abruptly rise to a higher dielectric plateau, which may be in connecting with this activation energy.

To further promote the industrial application of this studied CP materials system, multilayer ceramic are prepared through the conventional tape casting process, consisting of 8 active x = 0.04 SNSYTZO ceramic layers with each layer approximate 50 μm and an area approximate 6.25 mm^2, as the displayed SEM image in Fig. 6 a. The ceramic active layer shows high density and low porosity, and no abnormal grain growth, ceramic crack, and delamination are found, mainly due to the high quality of uniform nanometre starting powder. Meanwhile, Fig. 6 b present the surface element overlapping mapping of x = 0.04 SNSYTZO ceramic, and Fig.6 c to i give the specific elemental mapping of (Pt, Ti, Zr, Sb, Nb, Sm, and Y), illustrating that these elements of this study materials system are homogeneously distributed into the active ceramic layers, and no elemental segregation appear. Also, the inner Pt electrodes show excellent continuation, and no transparent electrodes permeate to the active ceramic layer. Those morphology microstructure analysis added together indicate the high quality of the prepared x = 0.04 SNSYTZO multilayer ceramic.

To detect the electric behavior of the prepared multilayer ceramic, Fig. 7 a and b give its elaborate dielectric response versus temperature and frequency. The dielectric permittivity of this study's CP multilayer ceramic nearly shows the variation tendency of its ceramic. However, the dielectric permittivity in low-temperature range (−100 to 0 °C) of x = 0.04 SNSYTZO multilayer ceramic is higher and more stable than that of the same composition ceramic, as shown in Fig. 7 a. And the dielectric loss shows no prominent typical Debye relaxation peak around 10^5 Hz, corresponding to the no-show dielectric permittivity plateau. It is notable that the dielectric permittivity in the high-frequency range (10k to 1 M Hz) is higher than that of the same composition ceramic in the whole test temperature range, as given in Fig. 7 b. Surprisingly, the dielectric loss in full frequency and temperature range present much lower value and reach to 0.02 at 10K Hz under −100 °C. Consequently, the x = 0.04 SNSYTZO multilayer ceramic prefers a better dielectric performance compared with its ceramic state, which may result from the advantage of tape-casting preparation techniques. When the bias up to −10 V, the electric diploe decrease its activity so that the dielectric permittivity decrease and dielectric loss increase, a typical Debye relaxation appear in the high frequency (> 10^5 Hz) range.

Considering the requirement of practical dielectric capacitor application, stable dielectric permittivity and loss under bias could ensure the stability of the electronic devices [32], Fig. 7 c and d give the dielectric response versus bias under variation frequency at room temperature. The dielectric permittivity and loss show a very stable tendency in the bias range from −10 to 10 V, as shown in Fig. 7 c and d. It is remarkable that the dielectric loss slightly goes up at low frequency (100 Hz) with increasing bias fields from 8 to 10 V, as illustrated in Fig. 7 c. And Fig. 7 d also show a little fluctuation above 4 × 10^5 Hz frequency under −10 V bias fields. The dielectric performance

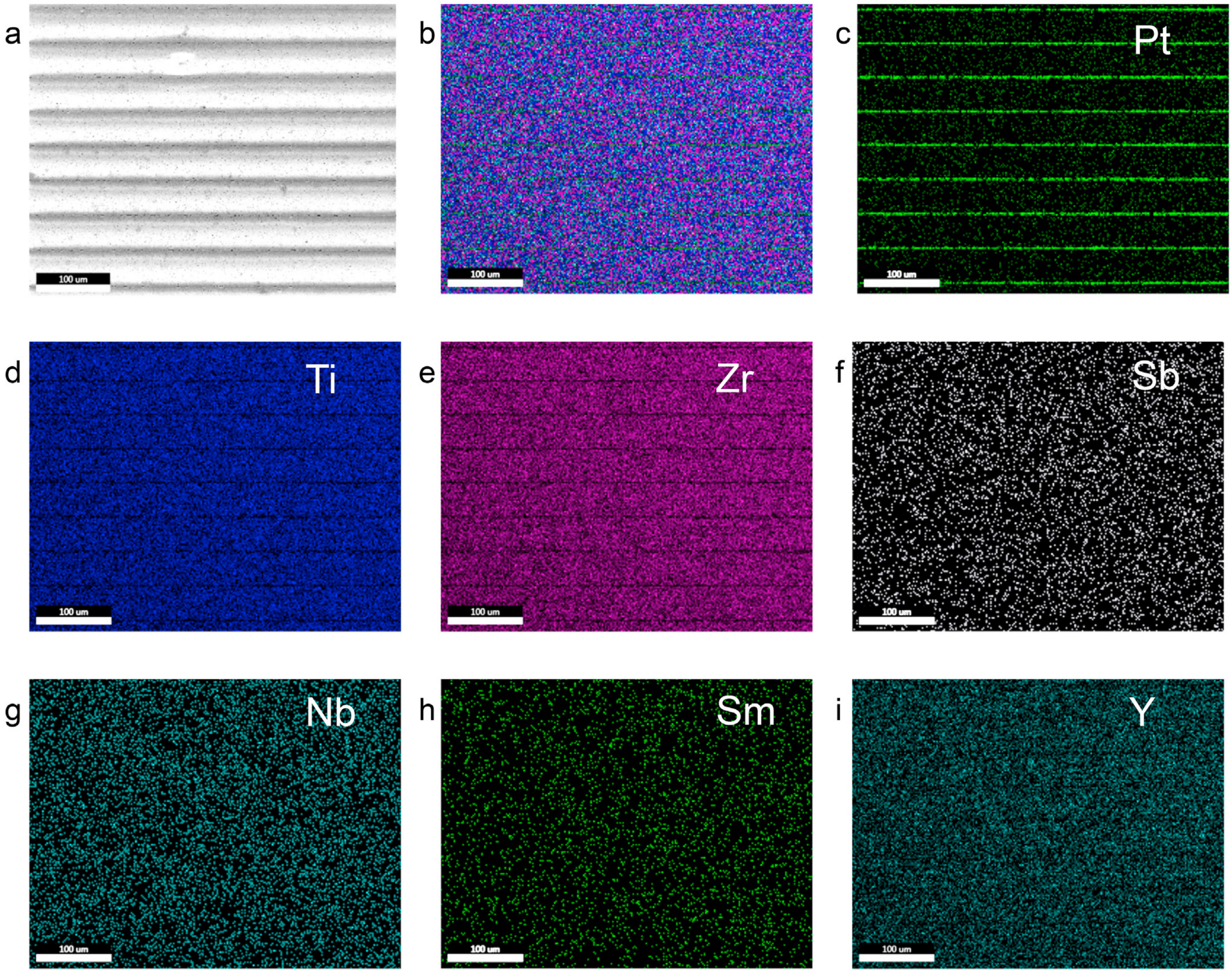

Fig. 6. (a) SEM image of x = 0.04 SNSYTZO multilayer ceramic. (b) Energy-dispersive X-ray spectroscopy (EDX) mapping of all elements overlapping (c) to (i) are the EDX mapping image of each element (Pt, Ti, Zr, Sb, Nb, Sm, and Y).

deterioration of both positons under high bias could be associated with the leakage current effect cross the 50 μm active layer [33].

4. Conclusion

In this study, double pentavalent (Sb^{5+}, Nb^{5+}) and trivalent (Sm^{3+}, Y^{3+}) co-doped $Ti_{0.9}Zr_{0.1}O_2$ (SNSYTZO, x = 0.01–0.20) were first prepared through the conventional solid-state method. XRD results prove that ceramics under x = 0.04 show a perfect rutile phase with the tetragonal crystal structure. However, minor brookite orthorhombic crystal structure appears when $x > 0.04$. SEM images present that the mean grain size of SNSYTZO ceramic slightly reduces from 30 μm to 23μm with increasing doping ions due to the conventional ions pinning effect impeding the mobility of grain boundary during the high-temperature sintering process. Meanwhile, the SD of grain size distribution decrease from the value of 12 to 5 associated with the secondary phases pinning effect. The dielectric loss of x = 0.04 SNSYTZO ceramic slightly achieves 0.1; simultaneously, the dielectric permittivity could keep 2.8×10^4, whose dielectric response shows excellent temperature- and frequency stability. And the complex modulus test excludes the conductivity process hides in a dielectric relaxation behavior. The impedance spectrum displays two kinds of activation energies 0.48 eV and 0.089 eV for high and low-temperature regions, respectively. The 0.089 eV of this studied ceramic could be attributed to the intrinsic electron traps in shallow potential due to the electron pinning effect, and the 0.48 eV is associated with oxygen vacancy or an interfacial process. Then x = 0.04 SNSYTZO material system is chosen to prepare multilayer ceramic through the conventional tape casting to investigate dielectric response further. The dielectric loss of x = 0.04 SNSYTZO multilayer ceramics could reach 0.02, keeping the dielectric permittivity up to 10^5. Additionally, the dielectric behaviors are very stable tendencies in the bias range from −10 to 10 V, and it is valuable for the potential supercapacitor and is key to the miniaturization and integration of electronics. The double pentavalent and trivalent co-doped strategies could be useful for the design of new classes of such CP materials from the purely scientific point of view. It could be applied to a wide range of other functional materials systems, such as lead-based/lead-free piezoelectric materials to regulate their piezoelectric constant and operation temperature, ferroelectric/antiferroelectric energy storage materials to tune their energy storage density and energy storage efficiency, electrocaloric materials to adjust their temperature stability and maximum exothermic value, and so on.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

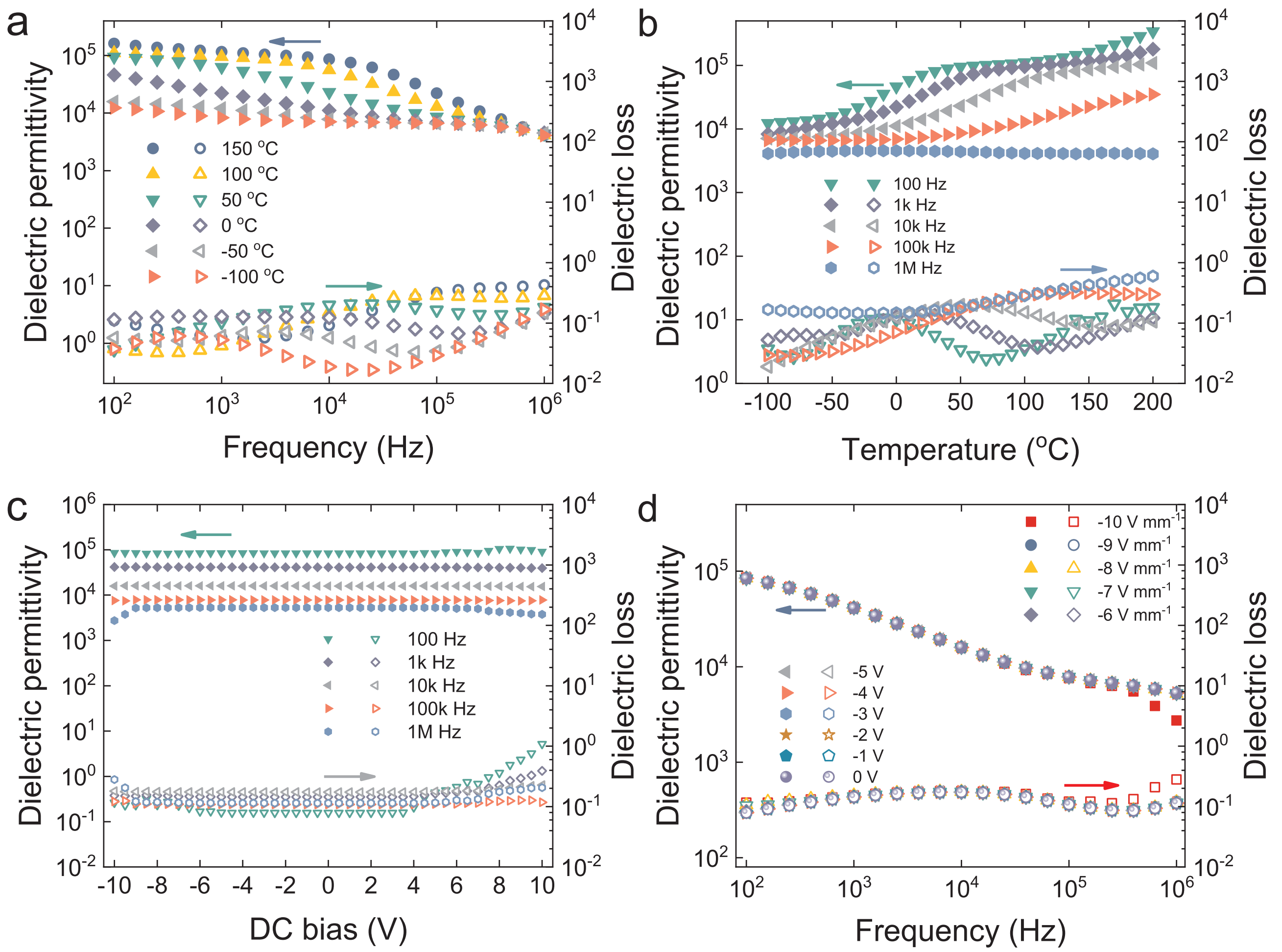

Fig. 7. (a) The dielectric permittivity and loss as a function of frequency with the selected temperature (−100, −50, 0, 50, 100, and 150 °C) for $x = 0.04$ SNSYTZO multilayer ceramic. (b) The dielectric permittivity and loss versus temperature with the selected frequency (100, 1k, 10k, 100k, and 1 M Hz). (c) The dielectric permittivity and loss for $x = 0.04$ SNSYTZO multilayer ceramic vs bias electric fields range from −10 to 10 V mm^{-1} under the selected frequency. (d) The dielectric permittivity and loss vs. frequency range from 100 to 1 M Hz under the selected bias electric fields. The bias dielectric response test is carried out at room temperature.

Acknowledgements

This work was supported by the National Nature Science Foundation of China-NSAF under Grant 51802182, 51972263, and 21473130, Shaanxi Province Nova Program of Science and Technology (Grant No. 2018KJXX-081), 2019 CAST Innovation Foundation of China, and in part by Fundamental Research Funds for the Central University (xjh012019025). Authors also thank the support of the Natural Science Foundation of Shaanxi Province under Grant 2020JM-004.

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